# Effect of Source Inductance on MOSFET Rise and Fall Times

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## *Abstract*

The need for advanced MOSFETs for DC-DC converters applications is growing as is the push for applications miniaturization going hand in hand with increased power consumption. These advanced new designs should theoretically translate into doubling the average switching frequency of the commercially available MOSFETs while maintaining the same high or even higher efficiency.

MOSFETs packaged in SO8, DPAK, D2PAK and IPAK have source inductance between 1.5 nH to 7 nH (nanoHenry) depending on the specific package, in addition to between 5 and 10 nH of printed circuit board (PCB) trace inductance. In a synchronous buck converter, laboratory tests and simulation show that during the turn on and off of the high side MOSFET the source inductance will develop a negative voltage across it, forcing the MOSFET to continue to conduct even after the gate has been fully switched off.

In this paper we will show that this has the following effects:

- The drain current rise and fall times are proportional to the total source inductance (package lead + PCB trace)
- The rise and fall times arealso proportional to the magnitude of the drain current, making the switching losses nonlinearly proportional to the drain current and not linearly proportional as has been the common wisdom
- It follows from the above two points that the current switch on/off is predominantly controlled by the traditional package's parasitic inductance and to a lesser degree by the MOSFET parameters. This means that switching speeds have reached a limiting factor in the form of the total source inductance
- Lab tests show that during turn off, the MOSFET will behave as a current source leading to further deterioration of the losses
- The above points explain why measured switching losses have always been higher than those calculated by textbook equations
- Improvements in MOSFET parameters like gate-drain charge, Qgd, will not fully translate into improvements in DC-DC converter performance as long as we continue to use inadequate packages and PCB layout techniques
- Some modern packages like BGA and DirectFet have addressed this point and possess very little source inductances

We will demonstrate that the results obtained in this paper are supported by simulation and lab test results.

## *Detailed Mathematical Approach*

Figure 1b depicts a typical DPAK MOSFET package used in the power conversion field. This class of packages which also includes D2PAK, IPAK and TO-220, has been in use for a long time and has been the work horse of the industry. Modern electronics and in particular personal computers (PCs), notebook computers and the myriad of handheld electronic devices have always required a continuous increase in power, features and functionality from the DC-DC converters used while allowing for an ever diminishing PCB real estate. This has pushed the switching frequencies to the levels they are at today - i. e. from 200 KHz to 2 MHz - to facilitate the physical shrinkage of the PCB space taken by them. As we will demonstrate below, this increase in switching frequency can cause problems that lead to excessive power loss, lower efficiency and higher temperature operation leading to lower reliability.

## *1. MOSFET Turn Off*

Figure 1a depicts the control MOSFET in a synchronous buck converter equivalent circuit as it turns off. In order to write the equations that govern the drain current turn off we will use the representations shown in Figure 2 to help explain what happens inside the MOSFET. We have represented the gate threshold voltage as a simple battery of value *Vgth* typically between 0.8 and 3 V.

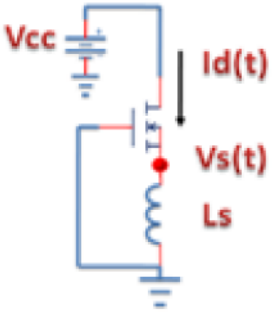



**Figure 1a.** Simplified Circuit Schematic depicting the MOSFET t turn off, *tf*.

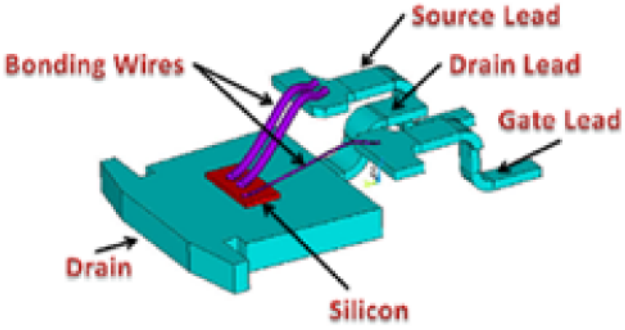



**Figure 1b.** Power package showing the source lead and bonding wires that for the source inductance, *Ls*.

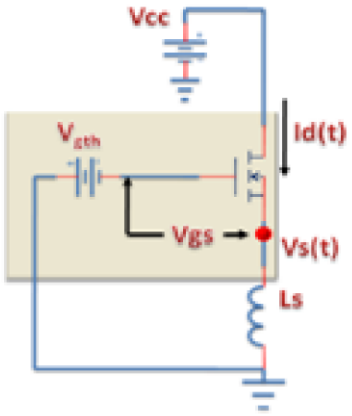



**Figure 2.** Gate-Source Loop Parameters.

The relationship between the transconductance, *gm*, the gate-source voltage, *Vgs,* and gate threshold voltage, *Vgth,* may be written as $gm := a \cdot (Vgs(t) - Vgth)$ where **a** is a basic MOSFET parameter which may be easily derived from Figures 3 and 4 below.

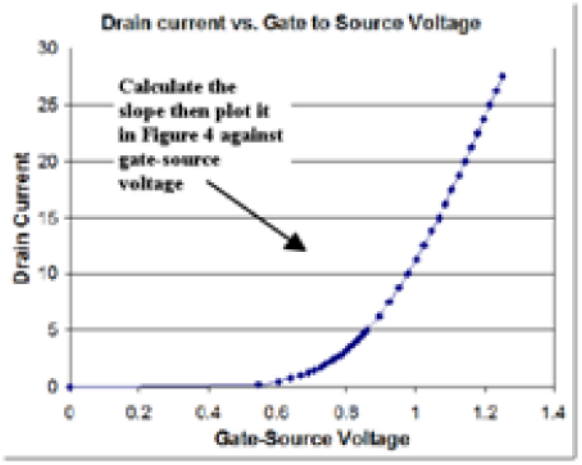



**Figure 3.** Gate-source transfer characteristics. By taking the slope at different gate-source voltages, we get the graph in Figure 4.

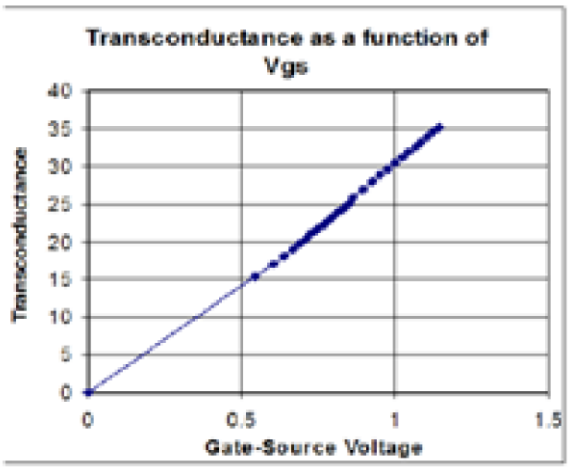



**Figure 4.** Forward transconductance as a function of gate-source voltage. The slope of this line is the parameter **a**.

With the aid of the circuit in Figure 1, one may write the equations:

$ea := Id(t) = gm \cdot Vgs(t)$

$$Id(t) = gm\ Vgs(t) \tag{1}$$

$eb := Vgs(t) = Vs(t) - Vgth$

$$Vgs(t) = Vs(t) - Vgth \tag{2}$$

$ec := gm = a \cdot Vgs(t)$

$$gm = a\ Vgs(t) \tag{3}$$

$subs(gm = a \cdot Vgs(t), ea)$

$$Id(t) = a\ Vgs(t)^2 \tag{4}$$

$subs(Vgs(t) = Vs(t) - Vgth, \%)$

$$Id(t) = a\ (Vs(t) - Vgth)^2 \tag{5}$$

$solve(\mathbf{(5)}, Vs(t))$

$$\frac{a\ Vgth + \sqrt{a\ Id(t)}}{a}, \ -\frac{-a\ Vgth + \sqrt{a\ Id(t)}}{a} \tag{6}$$

$$e0 := Id(t) + 1/Ls \cdot \int \frac{a\ Vgth - \sqrt{a\ Id(t)}}{a}\ dt$$

$$Id(t) + \frac{\int \frac{a\ Vgth - \sqrt{a\ Id(t)}}{a}\,dt}{Ls} \tag{7}$$

$e00 := Id(t) + 1/Ls \cdot \int \frac{a\ Vgth + \sqrt{a\ Id(t)}}{a}\,dt$

$$Id(t) + \frac{\int \frac{a\ Vgth + \sqrt{a\ Id(t)}}{a}\,dt}{Ls} \tag{8}$$

$e1 := \frac{d}{dt}\ e00$

$$\frac{d}{dt}\ Id(t) + \frac{a\ Vgth + \sqrt{a\ Id(t)}}{Ls\ a} \tag{9}$$

$sol := dsolve(\{e1, Id(0) = IL\}, Id(t))$ :

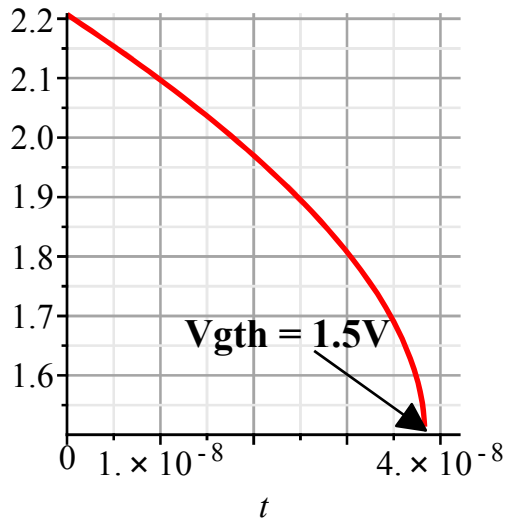
$Idt := eval(Id(t), sol)$ :

$tf := solve(Idt = 0, t)$ : $Vst := \frac{a\ Vgth + \sqrt{a\ Idt}}{a}$ :

where *Idt* is the drain current as a function of time *t*, *tf* is the drain current fall time as a function of a drain current *IL* and the circuit parameters, and *Vst* is the MOSFET source voltage as a function of time *t*.

Using the above equations in *Idt* and *Vst* we can now explore the different influences of the MOSFET and circuit parameter on the fall time *tf*.

$plot(evalf(subs(Vgth = 1.5, a = 30, Ls = 5 \cdot 10^{-9}, IL = 15, Vst)), t = 0 .. 4.2 \cdot 10^{-8}, thickness = 2, gridlines)$




$plot(evalf(subs(Vgth = 1.5, a = 30, Ls = 5 \cdot 10^{-9}, IL = 15, Idt)), t = 0 ..4.2 \cdot 10^{-8}, thickness = 2, gridlines)$

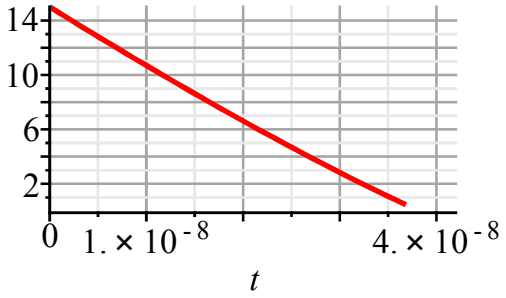
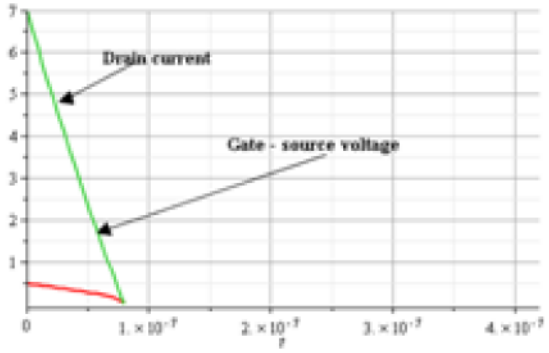


**Figure 5.** The voltage across the source inductor as a function of time *t*.

**Figure 6.** The drain (or inductor) current as a function of time *t*.

$$plot(\{evalf(subs(Vgth=1, a=30, Ls=15\cdot10^{-9}, IL=7, (Vst-Vgth))), evalf(subs(Vgth=1, a=30, Ls=15\cdot10^{-9}, IL=7, Idt))\}, t=0..4.2\cdot10^{-7}, thickness=2, gridlines)$$

$$plot(\{evalf(subs(Vgth=1, a=30, Ls=15\cdot10^{-9}, IL=40, (Vst-Vgth))), evalf(subs(Vgth=1, a=30, Ls=15\cdot10^{-9}, IL=40, Idt))\}, t=0..4.2\cdot10^{-7}, thickness=2, gridlines)$$



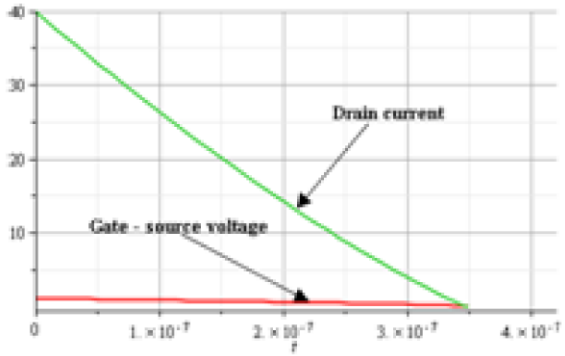
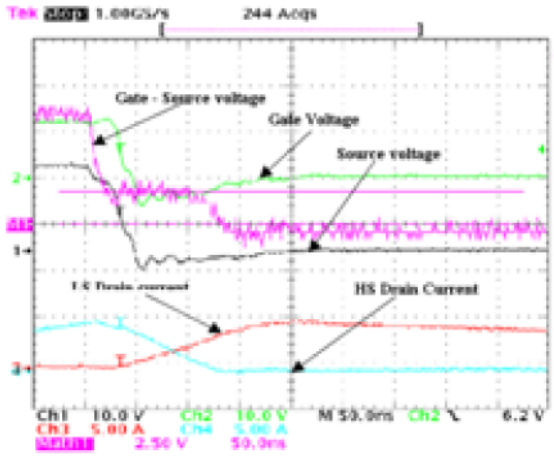




**Figure 7.** Drain current and gate-source voltage for initial current = 7 A

**Figure 8.** Drain current and gate-source voltage for initial current = 40 A

The above two plots show very clearly the very strong dependency of the fall time *tf* on the initial current. A larger initial current results in a larger fall time *tf*. This observation is confirmed by the lab test results in Figures 9 and 10 below.



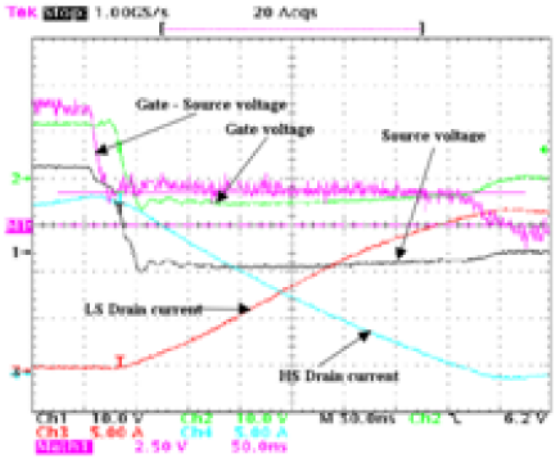




**Figure 9.** Captured scope image showing the control and synchronous rectifier currents, gate voltage, source voltage and gate-source voltage for low initial current ≈ 7 A in a synchronous buck converter

**Figure 10.** Captured scope image showing the control and synchronous rectifier currents, gate voltage, source voltage and gate-source voltage for high initial current ≈ 40 A in a synchronous buck converter

Figures 9 and 10 depict the results of actual lab tests done on a synchronous buck converter where currents for both the high side and low side MOSFETs are shown together with the gate-source

voltage of the high side MOSFET and the switching node. Figure 11 depicts the simulation results using a very powerful device simulation software for two source inductance, *Ls*, values of 1nH and 10nH which clearly agree with both the mathematical formulae derived here and the lab test results.

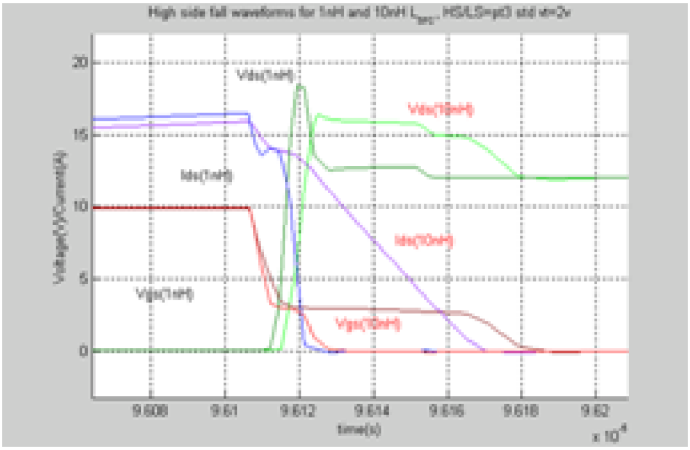



**Figure 11.** This graph depicts simulation results using device simulation software. This also agrees with the lab test and mathematical solution.

Figures 12 through 14 show the fall time, *tf*, as a function of different parameters using equation 10. There is a very strong nonlinear dependency of *tf* on the initial current, *IL*, the source inductance, *Ls*, and gate threshold voltage *Vgth*. The value of *tf* is independent of the converter's switching frequency making it a more substantial percentage of the duty cycle as the switching frequency goes higher resulting in higher power dissipation and lower efficiency.

$$plot3d\left(evalf\left(subs\left(\ a=30,\ \ Ls=10\cdot10^{-9},\ tf\right)\ \right),\ \mathrm{IL}=3\ ..40,\ \mathrm{Vgth}=0.5\ ..\ 6,\ axes=normal\right)$$

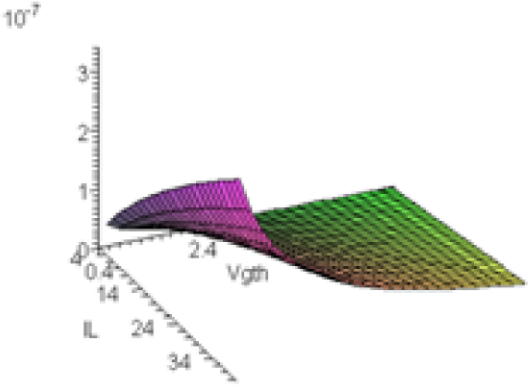



**Figure 12.** The current fall time, *tf,* as a function of initial current and gate threshold voltage. Notice the clear nonlinear dependency.

$$plot3d\left(evalf\left(subs\left(Vgth=1.5,\ a=30,\ \ Vgth=1,\ tf\right)\right),\ IL=3\ ..40,\ Ls=0.5\ 10^{-9}\ ..\ 15\ 10^{-9},\ axes=normal\right)$$

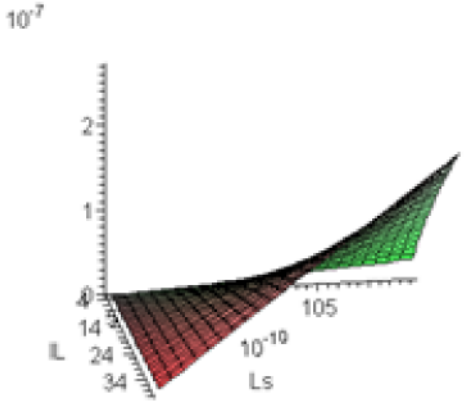



**Figure 13.** The current fall time, *tf* as a function of the source inductance and initial current. Again, clear nonlinear dependency.

$$plot3d(evalf(subs(a=30,\ IL=40, tf)),\ \mathrm{Ls}=0.1\ 10^{-9}..15\ 10^{-9},\ \mathrm{Vgth}=0.5\ ..\ 6,\ axes=normal)$$

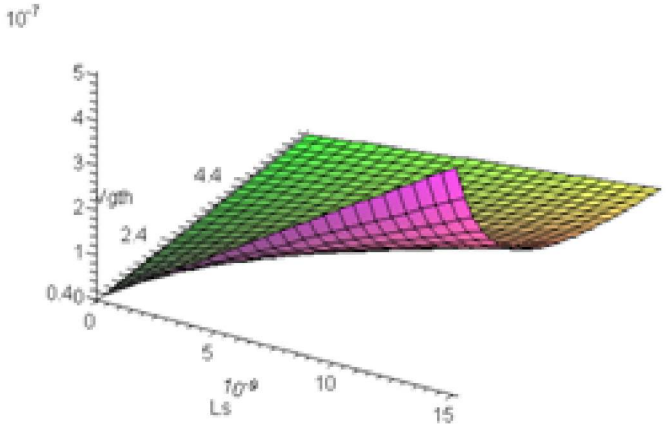



**Figure 14.** The current fall time, *tf*, as a function of gate threshold voltage and source inductance. Similar plots and/or calculations may help the designer in the choice of a MOSFET's silicon and package

For completeness, it is worthwhile noting that the following approximations have been done to be able to obtain an exact

symbolic solution that can help us understand the dependencies of the current fall time, *tf*, on the different parameters where the following parameters have been ignored:

**1.** The effect of the equivalent source resistance, ESR, of the inductor *Ls* since it is in the range of one or two milliohms

**2.** The effect of gate-source capacitance, Cgs, and the gate-drain capacitance, Cds

**3.** The effect of the driver output impedance

**4.** The effect of the intrinsic gate resistance

**5.** The effect of the gate trace inductance

## 2. MOSFET Turn On

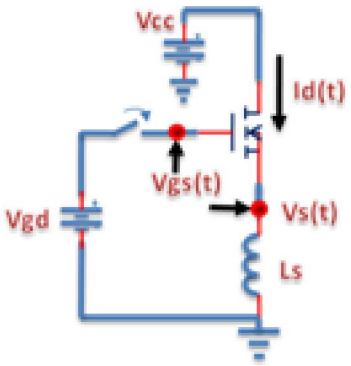



**Figure 15.** Simplified schematics used for the current turn on time calculation.

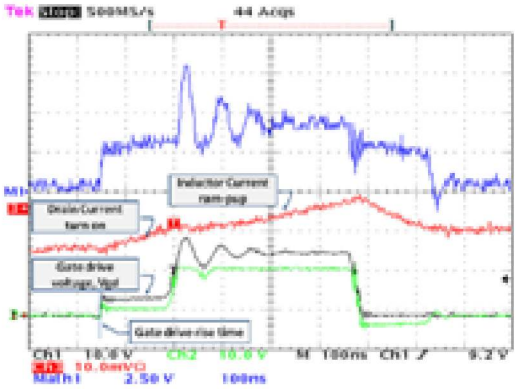


**Figure 16.** Lab test graph showing MOSFET turn on followed by inductor current ramp.

For the derivation of a closed form equation for the drain current turn on time we will use the simplified schematic in Figure 15. In this analysis we started with the full gate voltage applied to the drain assuming the rise time ≈ 0. This assumption is a very reasonable one as can be seen in Figure 16. This also allows the derivation of a closed form formulae for all currents and voltages. Figure 16 depicts captured scope images showing the gate drive, drain current and drain-source voltages.

$$Id(t) = \frac{1}{Ls}\int Vs(t)\,\mathrm{d}t :$$

$$Vgd = Vgs(t) + Vs(t) :$$

$$Id(t) = a\,(Vgs(t) - Vgth)^2 :$$

$$e0 := Id(t) = a\,(Vgd - Vs(t) - Vgth)^2$$

$$Id(t) = a\,(Vgd - Vs(t) - Vgth)^2 \tag{10}$$

$$e1 := \frac{1}{Ls}\int Vs(t)\,\mathrm{d}t = a\,(Vgd - Vs(t) - Vgth)^2$$

$$\frac{\int Vs(t)\,\mathrm{d}t}{Ls} = a\,(Vgd - Vs(t) - Vgth)^2 \tag{11}$$

$$e2 := \frac{\mathrm{d}}{\mathrm{d}t}\,e1$$

$$\frac{Vs(t)}{Ls} = -2\,a\,(Vgd - Vs(t) - Vgth)\left(\frac{\mathrm{d}}{\mathrm{d}t}\,Vs(t)\right) \tag{12}$$

$$sol := dsolve(\{e2, Vs(0) = Vgd - Vgth\}, Vs(t))$$

$$Vs(t) \tag{13}$$

$$= e^{\frac{1}{(Vgd - Vgth)\,a\,Ls}\left(-\mathrm{LambertW}\left(\right.\right.}$$

$$-\frac{e^{-\frac{1}{2}\,\frac{t}{Ls\,a\,(Vgd-Vgth)}+\frac{\ln(Vgd-Vgth)\,Vgd-\ln(Vgd-Vgth)\,Vgth-Vgd+Vgth}{Vgd-Vgth}}}{Vgd-Vgth}\Bigg)\,Ls\,a\,Vgd+\text{LambertW}\Bigg($$

$$-\frac{e^{-\frac{1}{2}\,\frac{t}{Ls\,a\,(Vgd-Vgth)}+\frac{\ln(Vgd-Vgth)\,Vgd-\ln(Vgd-Vgth)\,Vgth-Vgd+Vgth}{Vgd-Vgth}}}{Vgd-Vgth}\Bigg)\,Ls\,a\,Vgth-\frac{1}{2}\,t+(\ln(Vgd$$

$$-Vgth)\,Vgd-\ln(Vgd-Vgth)\,Vgth-Vgd+Vgth)\,Ls\,a\Bigg)$$

$Vst := eval(Vs(t), sol)$ :

$e3 := \frac{d}{dt}\,Id(t) = \frac{1}{Ls}\,Vst$

$$\frac{d}{dt}\,Id(t) \qquad \textbf{(14)}$$

$$= 1\,/$$

$$Ls\,e^{\frac{1}{(Vgd-Vgth)\,a\,Ls}\left(-\text{LambertW}\Bigg(-\frac{e^{-\frac{1}{2}\,\frac{t}{Ls\,a\,(Vgd-Vgth)}+\frac{\ln(Vgd-Vgth)\,Vgd-\ln(Vgd-Vgth)\,Vgth-Vgd+Vgth}{Vgd-Vgth}}}{Vgd-Vgth}\Bigg)\,Ls\,a\,Vgd+\text{LambertW}\Bigg($$

$$-\frac{e^{-\frac{1}{2}\,\frac{t}{Ls\,a\,(Vgd-Vgth)}+\frac{\ln(Vgd-Vgth)\,Vgd-\ln(Vgd-Vgth)\,Vgth-Vgd+Vgth}{Vgd-Vgth}}}{Vgd-Vgth}\Bigg)\,Ls\,a\,Vgth-\frac{1}{2}\,t+(\ln(Vgd$$

$$-Vgth)\,Vgd-\ln(Vgd-Vgth)\,Vgth-Vgd+Vgth)\,Ls\,a\Bigg)$$

$sol2 := dsolve(\{e3, Id(0) = 0\}, Id(t))$ :

$Idt := eval(Id(t), sol2)$ :

$plot(subs(Vgth = 1.5,\ a = 30, Ls = 5\ 10^{-9}, Vgd = 12,\ Idt), t = 0..1.5\ 10^{-8}, gridlines)$

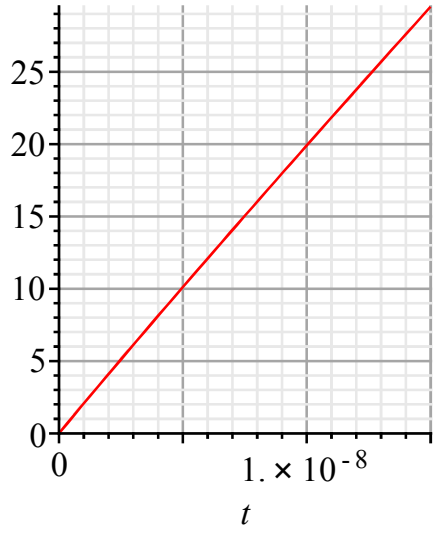



**Figure 16.** The drain current as a function of time *t*.

$plot3d(subs(Vgth = 1.5,\ a = 30, Vgd = 5,\ Idt), t = 0..2\ 10^{-8}, Ls = 0.1\ 10^{-9}..10^{-8}, axes = normal)$

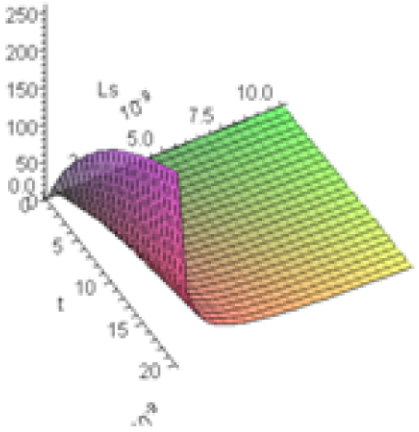



**Figure 17.** Current as a function of the source inductance *Ls* and time *t*.

$plot3d(subs(\ a = 30, Vgd = 5,\ Ls = 5\ 10^{-9},\ Idt), t = 0..2\ 10^{-8}, Vgth = 0.5..3, axes = boxed)$

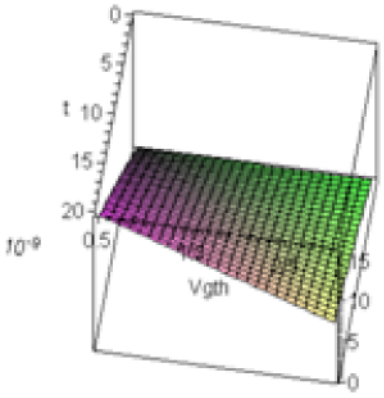



**Figure 18.** The drain current as a function of the gate threshold voltage and time

$plot3d(subs(\ Vgth = 1.5, Vgd = 5,\ Ls = 5\ 10^{-9},\ Idt), t = 0..2\ 10^{-8}, a = 1..100, axes = boxed)$

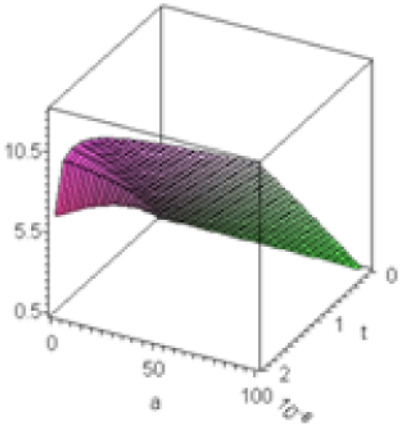



**Figure 19.** The drain current as a function of the parameter *a* and time

## *Derivation of on time, ton*

The on time, *ton*, can now be calculated by substituting *IL* in the drain current equation. This value represents the inductor or drain current in the synchronous buck converter at the time of turn on. When the equation was solved, we got two solutions *ton1* and *ton2*. Only *ton2* is the equation that represents the right solution. Figure 20 and equation 15 below were used to verify this conclusion.

$ton := solve((Idt) = IL, t)$ :

$ton1 := simplify(ton[1])$ :

$ton2 := simplify(ton[2])$ :

$plot(\{subs(Vgth = 1.5,\ a = 30, Ls = 5\ 10^{-9}, Vgd = 12,\ Idt), 20\}, t = 0..1.5\ 10^{-8}, gridlines)$

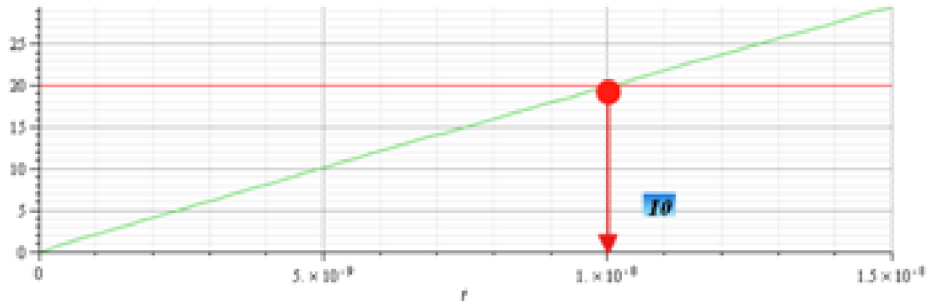



**Figure 20.** The drain current as a function of time *t*.

$evalf(subs(Vgth = 1.5, Vgd = 12, a = 30,\ Ls = 5\ 10^{-9}, IL = 20,\ (ton2)))$

$1.004824247\ 10^{-8}$ **(15)**

$plot3d(\ subs(Vgth = 1.5, Vgd = 5, a = 30, ton2), Ls = 10^{-9}..10^{-8}, IL = 5..40, axes = normal)$

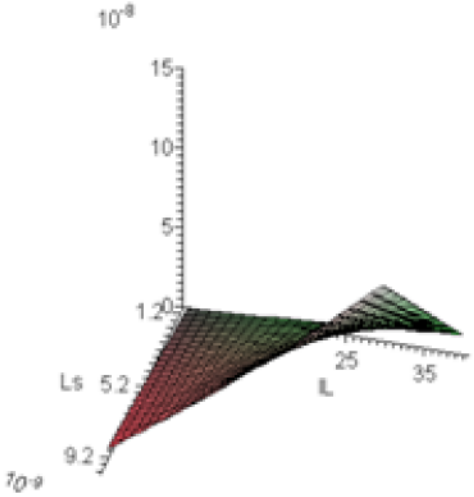



**Figure 21.** On time, *ton2*, as a function of inductor current *IL* and source inductance *Ls*.

$plot3d(\ subs(IL = 40, Vgd = 5, a = 30, ton2), Ls = 10^{-9}..10^{-8}, Vgth = 0.5..4, axes = normal)$

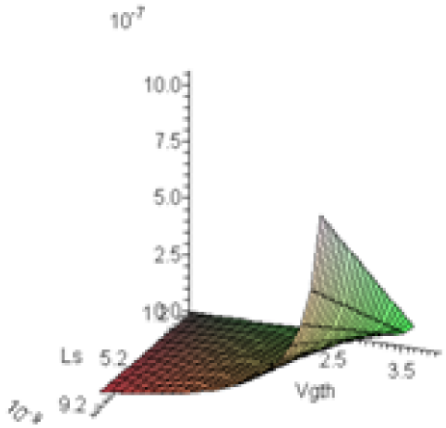



**Figure 22.** On time as a function of the source inductance *Ls* and gate threshold voltage *Vgth*.

# Conclusion

**1.** The parasitic source inductance controls the drain current rise and fall times. We have shown that a smaller inductance is better. In modern MOSFETs there is a minimum inductance dictated by the device package e.g. ≈ 1 nH for SO8 and more for DPAK and D2PAK. Though modern packages offer superior performance, improved PCB layout techniques are a must.

**2.** The non-linear dependency of *IL* on gate-source voltage - gate threshold voltage plays a major role in switching times. Lower *gm* around the gate threshold will result in faster fall times.

**3.** Gate threshold voltage plays a role in the rise and fall times. Higher *Vgth* will result in faster fall time but will result in slower rise time.

**4.** The use of a bipolar gate drive voltage that swings both positive to turn on and negative for turn off will result in faster *tf*.

**5.** Given all of the above, improvements in gate-drain charge, Qgd, alone will not result in any significant improvements in switching times if the source inductance is large enough to adversely affect the rise and fall times. In order to take full advantage of the improvements in Qgd we must have:

- PCB layout with minimum trace inductance
- MOSFET package with minimum source inductance

**6.** The rise time can be made faster with the proper gate drive voltage. Larger gate drive voltage will result in faster on times but will increase the gate drive losses $\approx Cgs\ Vgd^2\ fs$ where *fs* is the switching frequency and *Vgd* is the gate drive voltage.

**7.** The above conclusions should place designers on the right track to design DC-DC converters that can perform at the highest efficiency possible for a given specification.

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